MOXSYN®

C68MX11 CPU

General Description

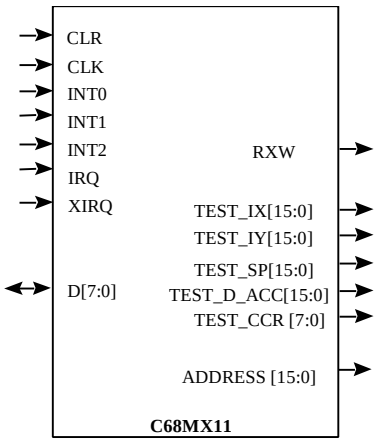
The C68MX11 CPU core is based on the Motorola M68HC11 microcontroller controller, but has an enhanced full 16 bit architecture, thus requiring less clock cycles for completing a large number of instructions compared with the original device. In addition to executing all M6800 and M6801 instructions, the C68MX11 instruction set includes more than 90 new opcodes as in the original M68HC11.

A large number of peripheral modules can be added to achieve highly sophisticated, on-chip capabilities, as for example a complete 16 bit timer system with 3 input capture lines, 5 output compare lines and real-time interrupt function, and an asynchronous or synchronous serial communication interface. Pins for complete monitoring of internal registers have been added for test purpose.

Features

- 16 bit architecture
- Machine code 100% compatible with M68HC11
- Byte efficient instructions, powerful addressing modes, 8x8 multiplication supported
- Less machine-cycles per operation
- Fully static logic implementation - clock frequencies from DC to MHz
- Memory mapped I/O
- Interrupt logic same as the M68HC11
- Default memory organization compatible with M68HC11 systems
- Address Space of 64 Kbytes
- Arbitrary number of external interrupts (5 in the default version)
- Scan logic available

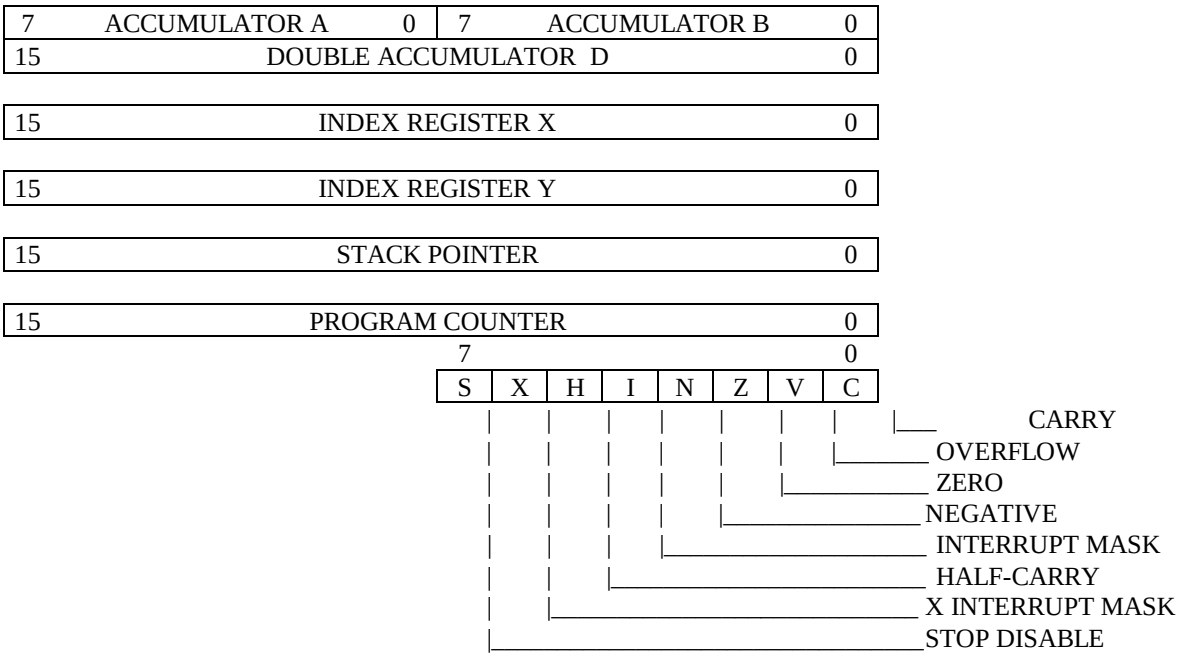
Symbol



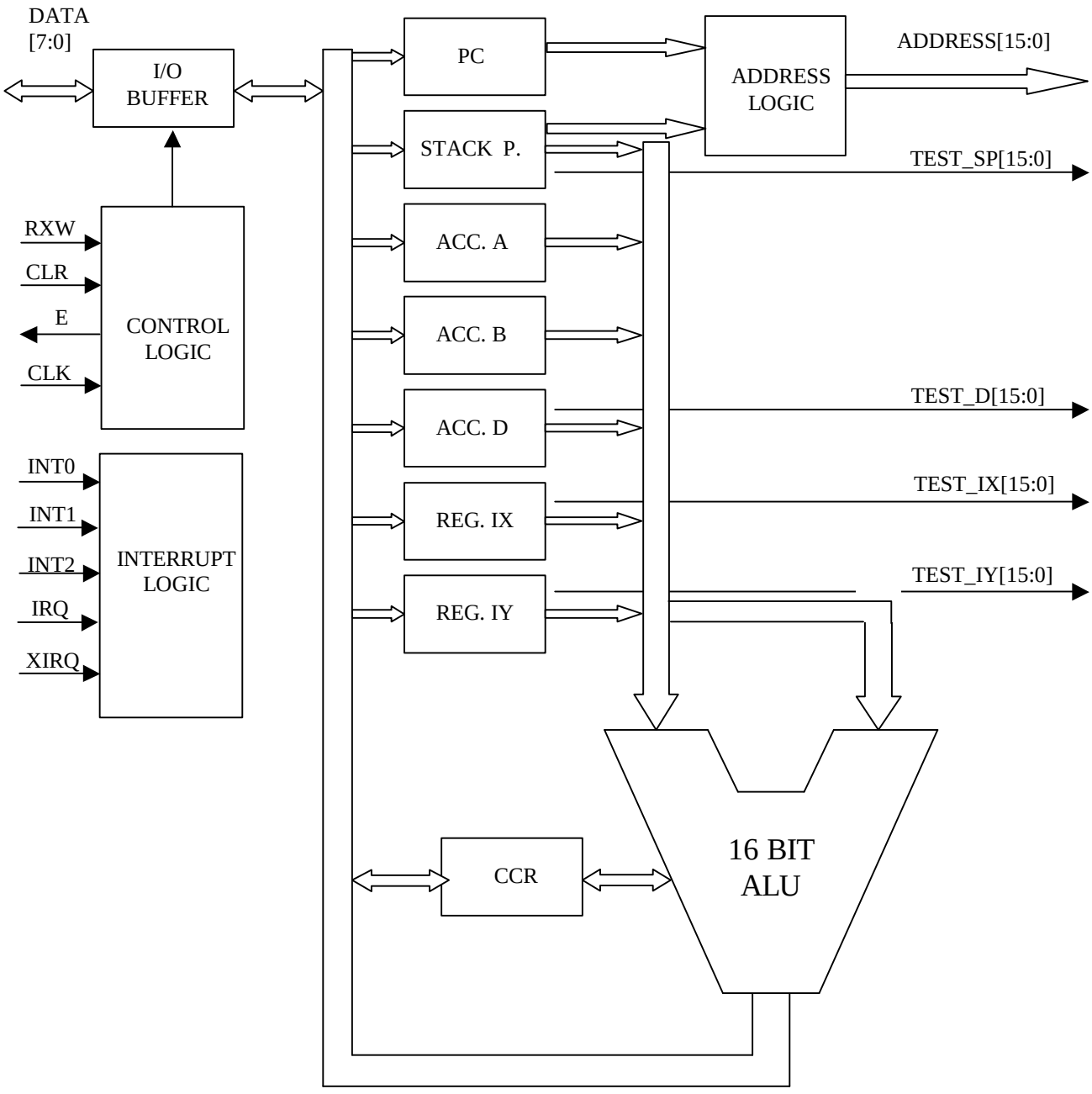
Pin Description

Name	Type	Polarity	Description
CLR	IN	Low	External reset
CLK	IN	-	Master clock
INT0n	IN	Low	Interrupt 0
INT1n	IN	Low	Interrupt 1
INT2n	IN	Low	Interrupt 2
IRQn	IN	Low	External Interrupt
XIRQ	IN	Low	Nonmaskable Interrupt
D[7:0]	INOUT	-	Data Bus
ADDRESS[15:0]	OUT	-	Address Bus
RXW	OUT		Read Write Control
Testing Interface Pins			
TEST_IX[15:0]	OUT	Low	Test Index Register IX
TEST_IY[15:0]	OUT	Low	Test Index Register IY
TEST_SP[15:0]	OUT	Low	Test Stack Pointer SP
TEST_D_ACC[15:0]	OUT	Low	Test Accumulator D
TEST_CCR[7:0]	OUT	Low	Test CCR Register

Programmer's Model

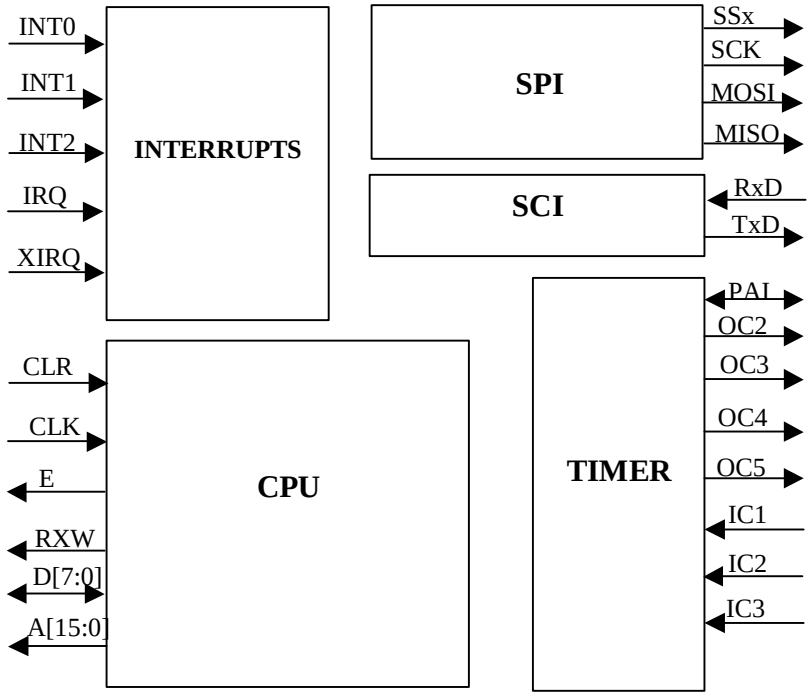


Block Diagram for CPU Core



CPU CORE

Block Diagram for C68MX11



C68MX11 Microcontroller

Functional description

The central processing unit (CPU) of the 68MX11 has more than 300 instruction opcodes and 6 addressing modes can be used to reference memory:

- IMM - **immediate** (the actual argument is contained in the byte(s) immediately following the instruction)
- DIR - **direct** (the least significant byte of the effective address of the instruction is contained in the byte following the opcode. The high-order byte of the effective address is assumed to be 00 hex)
- EXT - **extended** (the effective address explicitly appears in the 2 bytes following the opcode)
- IND - **indexed** (either index register IX or IY is used for effective address calculation)
- INH - **inherent** (the operands are CPU registers and they are inherently known by the CPU)
- REL - **relative** (used only for branch instructions)

The CPU is able of addressing 64 Kbytes of memory. I/O access is memory-mapped. Although the data busses have a width of 8 bit most of the instructions have 16 bit equivalent instructions. The C68MX11 offers multiply, add, subtract, compare, increment & decrement, load & store, and shift instructions of 16 bit operands. The CPU consists of two general-purpose 8-bit **accumulators** used to hold operands and results of arithmetic calculations or data manipulations. The accumulator A and B can be combined into a 16 bit double accumulator D. The 16 bit **index registers** IX and IY are used for indexed addressing modes. The CPU automatically supports a program stack. This stack may be located anywhere in the 64 Kbyte address space through the **stack pointer** and may be any size up to the amount of memory available in the system. The **condition code register (CCR)** contains five status indicators (carry, overflow, zero, negative, and the half carry flag), two interrupt masking bits (IRQ and XIRQ mask), and a STOP disable bit.

CORE Assumptions

The design is **fully synchronous** and doesn't contain any internal tristate buses, therefore special considerations for synthesis can be avoided. The design offers all of the original 308 opcodes and behaves exactly in the same manner as the original 68HC11,with the exception discussed below. Due to this modification the C68MX11 has actually 301 Opcodes

The variation from the original device are as following:

- The following OPCODES and relative mnemonics have been NOT implemented in order to save area or because they would have made no sense in the core implementation (TEST). If required they can be implemented on request.

  1. CPX IND,Y Opcode CD AC
  2. CPY IND,X Opcode 1A AC
  3. FDIV INH Opcode 03
  4. IDIV INH Opcode 02
  5. STOP INH Opcode CF
  6. TEST INH Opcode 00

CAST, Inc.
24 White Birch Drive
Pomona, New York 10907 USA

Phone: +1 914-354-4945
Fax: +1 914-354-0325
E-Mail: info@cast-inc.com
URL : www.cast-inc.com

The C68MX11 core is licensed from Moxsyn, S.r.l.