



Function Description

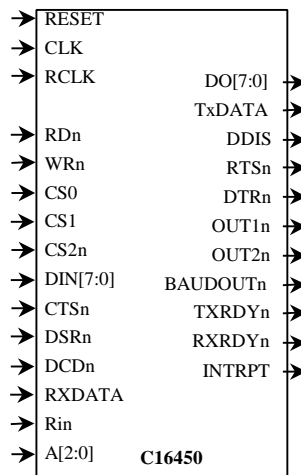
The C16450 programmable asynchronous communications interface (UART) core provides data formatting and control to a serial communication channel.

The core has select, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the core can transmit and receive serial data, supporting asynchronous operation.

Features

- ◆ Full double buffering
- ◆ Asynchronous operation
- ◆ Independently controlled Transmit, Line Status, Receive, and Data Set Interrupts
- ◆ Programmable data word length (5 - 8 bit), parity and stop bits
- ◆ Parity, overrun and framing error checking
- ◆ Supports up to 3 Mbps transmission rates (silicon dependent)
- ◆ Programmable Baud Rate Generator allows division of any reference clock by 1 to $(2^{16}-1)$ and generates an internal 16 X Clock
- ◆ False start bit detection
- ◆ Automatic break generation and detection
- ◆ Internal diagnostic capabilities
- ◆ Peripheral modem control functions
- ◆ The C16450 is available in VHDL or Verilog and synthesizes to approximately 2,000 gates depending on the process used

Symbol



C16450 Universal Asynchronous Receiver/Transmitter

Pin Description

Name	Type	Polarity	Description
RESET	In	High	External reset
CLK	In	-	Master clock
RCLK	In	-	Receive clock
RDn	In	Low	Read control
WRn	In	Low	Write control
CS0	In	High	Chip Select 0
CS1	In	High	Chip Select 1
CS2n	In	Low	Chip Select 2
DIN[7:0]	In	-	Data Input Bus
CTS _n	In	Low	Clear-to-Send
DSR _n	In	Low	Data Set Ready
DCD _n	In	Low	Data Carrier Detect
RXDATA	In	-	Receive Data
RI _n	In	Low	Ring Indicator
A[2:0]	In	-	Register Select
DO[7:0]	Out	-	Data Output Bus
TXDATA	Out	-	Transmit Data
DDIS	Out	High	Driver Disable
RTS _n	Out	Low	Request-to-Send
DTR _n	Out	Low	Data Terminal Ready
OUT1 _n	Out	Low	Output 1
OUT2 _n	Out	Low	Output 2
INTRPT	Out	High	Interrupt
BAUDOUT _n	Out	Low	Baud Out

Register description

The C16450 contains the following registers:

1. Line Control
2. Line Status
3. Interrupt Enable
4. Modem status
5. Modem Control
6. Transmitter Holding buffer
7. Receiver buffer
8. Interrupt Identification
9. Scratch

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Block Diagram

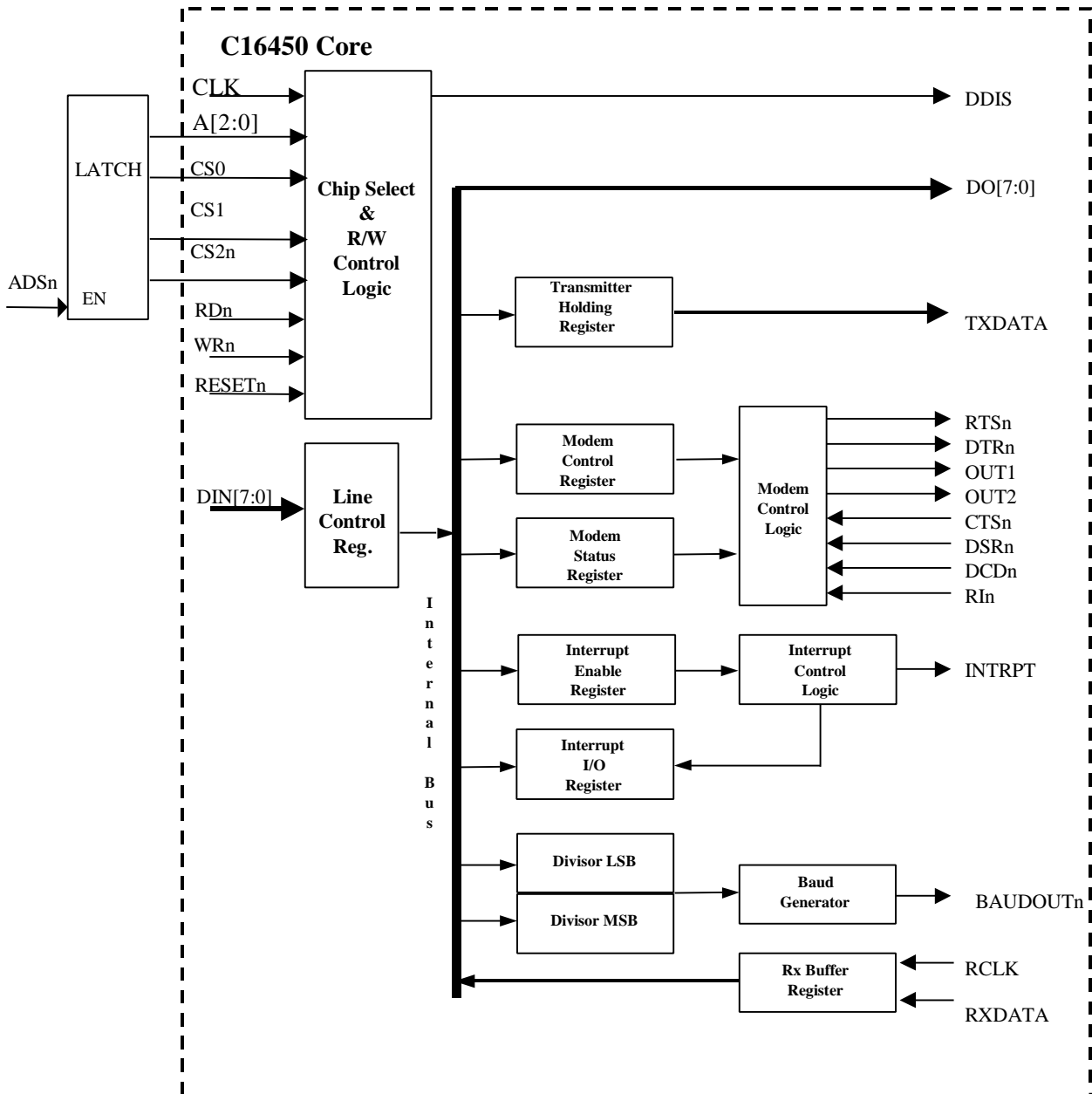


Figure 1: C16450 UART Block Diagram

C16450 Universal Asynchronous Receiver/Transmitter

Applications

- Serial data communications applications
- Modem interface

Functional Description

Line Control (LCR)

The Line Control Register is used to specify the data communication format. The break feature, parity, stop bits and word length can be changed by writing to the appropriate bits in LSR.

Line Status (LSR)

This register provides information on the status of data transfers between the C16450 and the CPU.

Interrupt Enable (IER)

The Interrupt Enable Register masks interrupts from the modem status registers, line status, transmitter empty and receiver ready to the INTRPT output pin.

Modem Status (MSR)

This register provides the current state of modem control lines.

Modem Control (MCR)

This register controls the interface lines with the MODEM and changes the status of the C16450 from normal operating mode and local loop-back mode (diagnostics mode).

Transmitter Holding Buffer

The transmitter section is composed of a Transmit Holding Register (THR) and a Transmit Shift Register (TSR). Writing to THR will transfer the contents of the data bus (DIN 7-0) to the Transmit Holding Register every time that the THR or TSR is empty. This write operation should be done when Transmit Holding Register Empty (THRE) is set.

Receiver Buffer

This register contains the assembled received data. On the falling edge of the start bit, the receiver section starts its operations. The start bit is valid if the RXDATA is still low at the middle sample of Start bit, thus preventing the receiver from assembling a false data character.

Interrupt Identification (IIR)

The Interrupt Identification Register provides the source of interrupt among four levels of prioritized interrupt conditions in order to minimize the CPU overhead during data transfers.

Scratchpad (SR)

This register stores the temporary byte for variable use.

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Core Assumptions

The functionality of the C16450 core was based on the Texas Instruments TL16C450. The following characteristics differentiate the C16450 from the Texas Instruments device:

- This core does not support connection of a crystal directly to the device. It was replaced by an external master clock signal (CLK).
- The bi-directional data bus has been split into two separate buses: DIN[7:0] and DO[7:0]. If required these buses can be combined into a single 8-bit bi-directional bus.
- The 1½ stop bit mode (for 5 bit word length) is not supported in this release.
- Signals rd2, wr2, xin, xout and csout have been eliminated from the interface (they can be added by request).
- Signal ADSn and address latch have been removed
- The register address is latched on the rising edge of the master clock (CLK).
- Divisor latch low (DLL), divisor latch high (DLM), THR register and SCR register are reset to all zeros.
- Both DLL and DLM registers must be loaded before BAUDOUTn has valid output.
- DO (output data bus) always shows the last selected register; after reset DO is "00".
- Reset requires at least one clock cycle.
- MSR register is reset during the clock cycle following a MSR read.
- Transmitter Empty status (TEMT), bit 6 of Line Status Register (LSR), is reset during the clock cycle following a TBR register write.
- Between 2 rising edges of WRn or RDn the core needs at least 2 clock (CLK) cycles. (Tcycle)

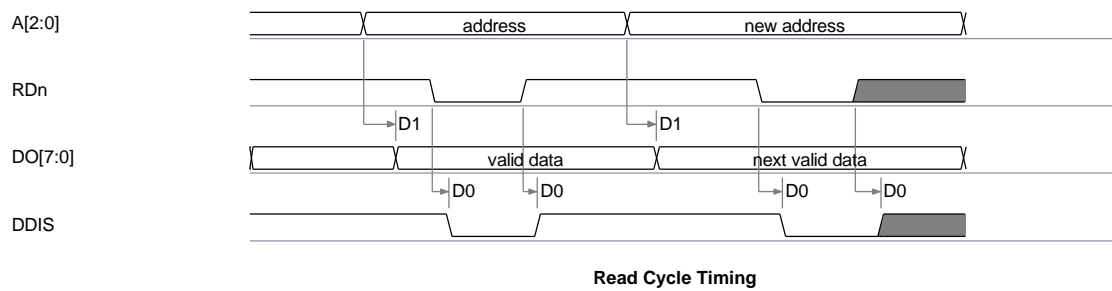
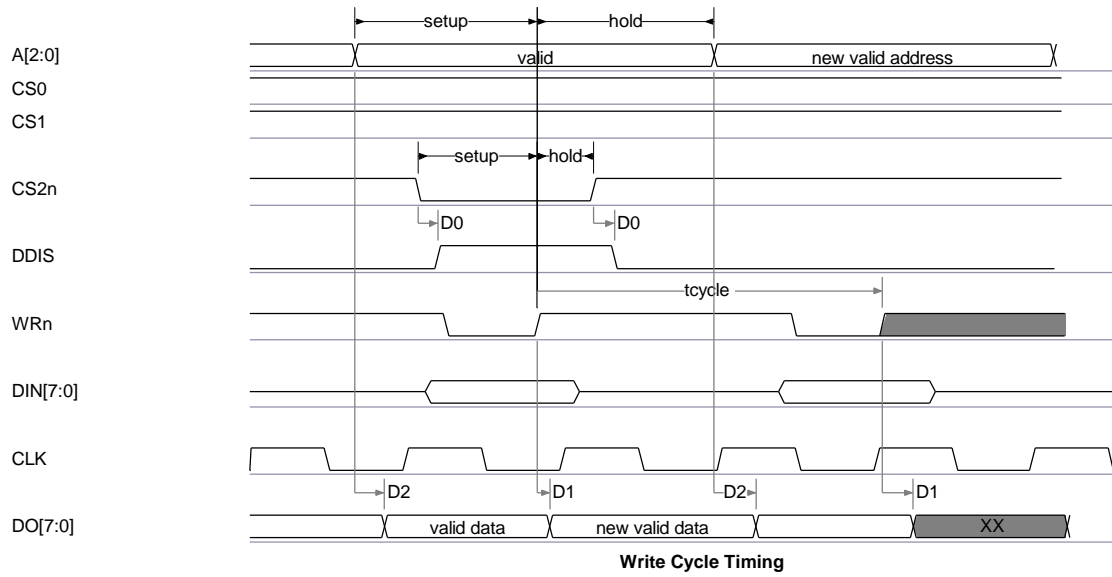
Timing variations differences from the Texas Instruments device:

Symbol	Parameter	C16450		TL16450	
		Min	Max	Min	Max
td ₁	Delay from WRn MCR to Output		tpd		100 nS
td ₂	Delay from MODEM Input to Set Interrupt		tpd		170 nS
td ₃	Delay from RDn to Reset Interrupt(RD MDR)		tpd after first CLK rising edge		140 nS
td ₄	Delay from WRn to Reset Interrupt(WR THR)		tpd		140 nS
td ₅	Delay from RDn to Reset Interrupt THRE (RD IIR)		tpd		140 nS
td ₆	Delay from initial INTR Reset to Transmit Start	1 Baudout Cycles	4 Baudout Cycles	8 Baudout Cycles	24 Baudout Cycles
td ₇	Delay from initial Write to Interrupt	4 Baudout Cycles	4 Baudout Cycles	16 Baudout Cycles	32 Baudout Cycles
td ₈	Delay from STOP to Interrupt (THRE)	1 CLK Cycle	1 CLK Cycle	8 Baudout Cycles	8 Baudout Cycles
td ₉	Delay from STOP to Set Interrupt		tpd		1RCLK Cycles
td ₁₀	Address, ADSn, Chip Select setup time [1]			15 ns	
td ₁₁	Address, ADSn, Chip Select hold time [1]			5 ns	

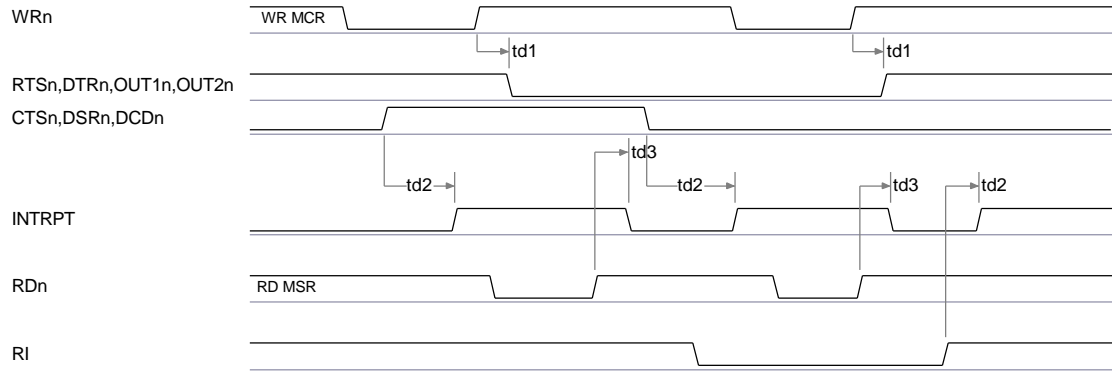
[1] Typical values: silicon dependent

C16450 Universal Asynchronous Receiver/Transmitter

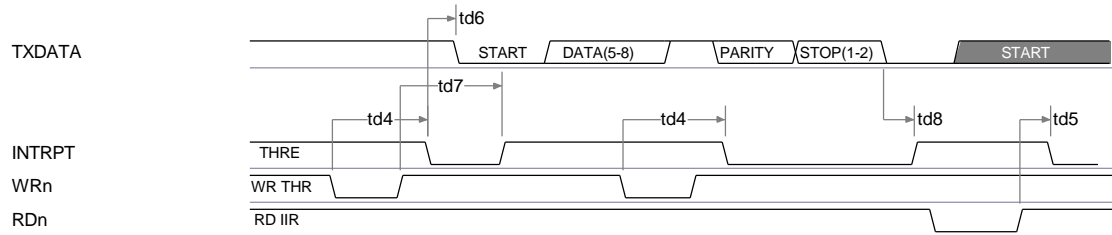
Timing Diagrams



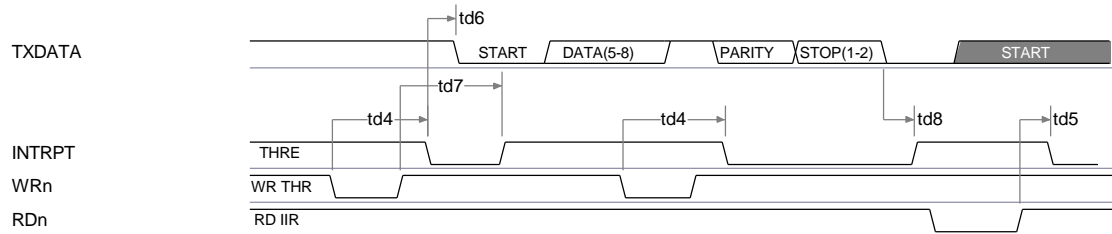
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MODEM Control Timing



Transmitter Timing



Transmitter Timing

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Supplied Files

readme.txt	General information about the core and installation
doc/	
C16450.pdf	This document
release.txt	Release notes
src/	
C16450.vhd	Top Level entity/architecture (VHDL version)
C16450.v	Top Level module (Verilog version)
tb/	
C16450ts.vhd	Testbench (VHDL version)
C16450tb.v	Testfixture (Verilog version)
C16450.stm	Stimulus file used by the testbench (VHDL version)
C16450.ref	Expected testbench results (VHDL version)
C16450_v.ref	Expected testbench results (Verilog version)
scripts/	
compile.do	Sample compilation script for ModelSim
simulatate.do	Sample simulation script for ModelSim
synopsys.scr	Sample Synopsys synthesis script for Synopsys

Testbench Notes (VHDL version)

The testbench provided can be used for functional and post-synthesis simulation, and is used to test the functionality of the core.

The stimulus file *C16450.stm*, and the expected results file *C16450.ref* must be in the local simulation directory.

Functional Simulation

Compile the *C16450.vhd* and the *C16450ts.vhd* files into a working library. Once the testbench is loaded into the simulator, simulate for 1300 us. At the end of the simulation the following message should appear:

"Note: test completed with no errors"

Post-Synthesis Simulation

If your synthesis tool renames the top level pins after routing, it may be necessary to create a dummy wrapper in order to use the supplied testbench.

Edit the file *C16450ts.vhd* and go to line 395 (SECTION 3) of testbench

Add the actual maximum expected delays of your silicon

Compile your post-synthesis or post-layout VHDL netlist file

Recompile the *C16450ts.vhd* file just edited

Simulate as above

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Textfixture Notes (Verilog version)

The textfixture provided can be used for functional and post-synthesis simulation, and is used to test the functionality of the core.

The expected results file *C16450_v.ref* should be in the local simulation directory.

Functional Simulation

Once the testfixture is loaded into the simulator, simulate for 1300 us. At the end of the simulation the following message should appear:

"Note: test completed with no errors"

Post-Synthesis Simulation

If your synthesis tool renames the top-level pins after routing, it may be necessary to create a dummy wrapper in order to use the supplied testfixture.

Edit the file *C16450tb.v* and go to line 895 of testfixture
Add the actual maximum expected delays of your silicon
Compile your post-synthesis or post-layout Verilog netlist file
Recompile the *C16450tb.v* file just edited
Simulate as above

Synthesis Notes

A Synopsys sample synthesis script is provided. The script will create a VHDL or Verilog gate-level netlist, and gate/performance reports at the completion of the synthesis process. It is recommended that a directory *syn* be created where the source files reside. The script expects to find all HDL source files in *../*. If this is not the case, then edit *C16450.scr* and update with the correct path.

Core Modifications

The C16450 core can be customized to include:

- Removal of internal baud rate generator
- Different CPU interface

Support

Every effort has been made to ensure that this core functions correctly. If a problem is encountered please contact MOXSYN:

Technical Support Hotline: +39-335-65-74-399

Fax: +39-736-43125

E-mail: <mailto:support@moxsyn.com>

URL: www.moxsyn.com

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Related Information

Data Transmission Circuits 1993 Data Book

Contact:

Texas Instruments
Literature Response Center
P.O. Box 809066
Dallas, Texas 75380-9066
URL: <http://www.ti.com>

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