

Function Description

The C6850 asynchronous communications interface (ACIA) megafunction provides data formatting and control to the asynchronous data communications of data bus systems.

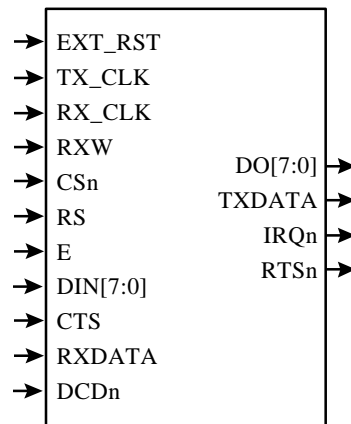
The megafunction has select, enable, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data.

In addition, a programmable control register provides the megafunction with a transmit control, a receive control, an interrupt control, variable word lengths and clock division ratios. Three control lines are provided for peripheral or modem operation.

Features

- ◆ Programmable data word length, parity and stop bits
- ◆ Parity, overrun and framing error checking instructions and counting loop interactions
- ◆ Supports transmission rates over the 1.0 Mbps spec
- ◆ False start bit deletion
- ◆ Peripheral modem control functions
- ◆ The C6850 was developed in VHDL and synthesizes to approximately 1,100 gates depending on the process used
- ◆ Functionality based on the Motorola MC6850

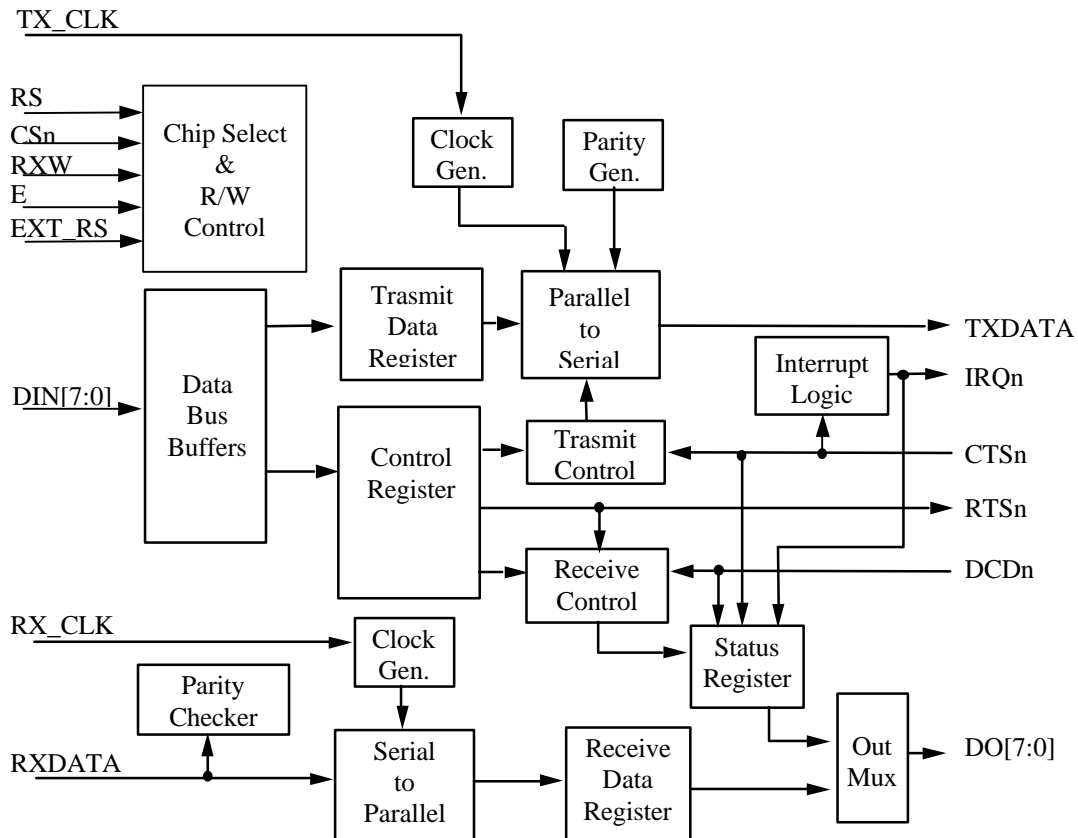
Symbol



Pin Description

Name	Type	Polarity	Description
EXT_RST	In	High	External reset
TX_CLK	In	-	Transmit clock
RX_CLK	In	-	Receive clock
RXW	In	-	Read /Write
CSn	In	Low	Chip Select
RS	In	Low	Register Select
E	In	-	Enable (clock)
DIN[7:0]	In	Low	Data Input Bus
RXDATA	In	-	Receive Data
CTS _n	In	Low	Clear-to -Send
DCD _n	In	Low	Data Carrier Detect
IRQ _n	Out	Low	Interrupt Request
TXDATA	Out	-	Transmit Data
RTS _n	Out	Low	Request-to-Send
DO[7:0]	Out	Low	Data Output Bus

Block Diagram



Applications

- Serial data communications applications
- Modem interface

Device Utilization & Performance

Target Device	Speed Grade	Utilization		Performance F_{max}	Availability
		LCs	EABs		
EPF7160	-10	118	-	29 MHz	Now
EPF9320	-15	153	-	29 MHz	Now
EPF6016	-2	185	-	38 MHz	Now
EPF8282	-2	185	-	25 MHz	Now
EPF10K10	-3	185	-	37 MHz	Now
EPF10K10A	-1	185	-	54 MHz	Now
EP1K30TC144	-1	174	-	95 MHz	Now

Deliverables

Encrypted Licenses

- Post-synthesis AHDL
- Assignment & Configuration
- Symbol file
- Include file
- Vectors for testing the functionality of the megafunction

VHDL Source Licenses

- VHDL RTL source code
- Testbench
- Example testbench wrapper for post-route simulation
- Vectors for testbench
- Simulation script
- Synthesis script
- Expected results for testbench

Verification Methods

The C6850 UART megafunction's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original Motorola 6850 chip, and the results compared with the megafunction's simulation outputs.

CAST, Inc.

24 White Birch Drive

Pomona, New York 10907 USA

Phone: +1 914-354-4945

Fax: +1 914-354-0325

E-Mail: info@cast-inc.com

URL : www.cast-inc.com

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