C16MX750
Universal Asynchronous Receiver/Transmitter with 64 FIFOs and Infrared (IrDA) Encoder/Decoder

Function Description

The C16MX750 programmable asynchronous communications interface (UART) megafunction provides data formatting and control to a serial communication channel.

The megafunction has select, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting asynchronous operation.

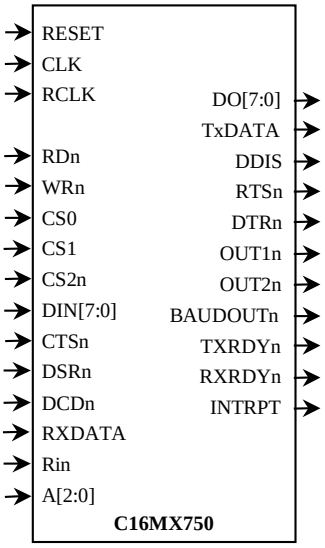
Features

- Capable of running with all existing 16450 and 16550A Software
- Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added or Deleted to or From the Serial Data Stream
- In FIFO mode, Transmitter and Receiver are each buffered with Programmable 16- or 64-Byte FIFOs to Reduce CPU Interrupts
- Programmable Auto- RTS\ and Auto- CTS\
- In Auto- CTS\ Mode, CTS\ Controls Transmitter
- In Auto- RTS\ Mode, Receiver FIFO Contents and Threshold Control RTS\
- Serial Ports Have Infrared Data Association (IrDA) Inputs and Outputs (OPTIONAL)
- Fully Programmable Serial Interface Characteristics:
    - 5-, 6-, 7-, or 8-Bit Characters
    - Even-, Odd-, or No-Parity Bit Generation and Detection
    - 1-, or 2-Stop Bit Generation
    - Baud Generation (DC to Silicon dependent Mbits Per Second)
- Parity, overrun and framing error checking

Features

- Supports up to 15 Mbps transmission rates (Typical value: silicon dependent)
- Programmable Baud Rate Generator allows division of any reference clock by 1 to (2^{16}-1) and generates an internal 16 X Clock
- False start bit detection
- Automatic break generation and detection
- Break, Parity, Overrun, Framing Error Simulation Peripheral modem control functions
- The C16MX750 was developed in VHDL/Verilog HDL and synthesizes to approximately 6,500 gates depending on the process used
- After Reset, All Registers Are Identical to the TL16C450 Register Set
- In the TL16C450 Mode, Hold and Shift Registers Eliminate the Need for Precise Synchronization Between the CPU and Serial Data
- Independent Receiver Clock Input
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Complete Status Reporting Capabilities
- Internal Diagnostic Capabilities:
    - o Loopback Controls for Communications Link Fault Isolation
    - o Break, Parity, Overrun, Framing Error Simulation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions (CTS\, RTS\, DSR\, DTR\, RI\, and DCD\)

Symbol



Applications

- Serial data communications applications
- Modem interface

Pin Description

Name	Type	Polarity	Description
RESET	In	High	External reset
CLK	In	-	Master clock
RCLK	In	-	Receive clock
RDn	In	Low	Read control
WRn	In	Low	Write control
CS0	In	High	Chip Select 0
CS1	In	High	Chip Select 1
CS2n	In	Low	Chip Select 2
DIN[7:0]	In	-	Data Input Bus
CTSn	In	Low	Clear-to -Send
DSRn	In	Low	Data Set Ready
DCDn	In	Low	Data Carrier Detect
RXDATA	In	-	Receive Data
RIn	In	Low	Ring Indicator
A[2:0]	In	-	Register Select
D0[7:0]	Out	-	Data Output Bus
TXDATA	Out	-	Transmit Data
DDIS	Out	High	Driver Disable
RTSn	Out	Low	Request-to-Send
DTRn	Out	Low	Data Terminal Ready
OUT1n	Out	Low	Output 1
OUT1n	Out	Low	Output 2
TxRDYn	Out	Low	Transmit ready
RxRDYn	Out	Low	Receiver ready
INTRPT	Out	High	Interrupt
BAUDOUTn	Out	Low	Baud Out

Register description

The C16MX750 contains the following registers:

1. Line Control
2. Line Status
3. Interrupt Enable
4. Modem status
5. Modem Control
6. Transmitter Holding buffer
7. Receiver buffer
8. Interrupt Identification
9. FIFO Control
10. Scratch

Block Diagram

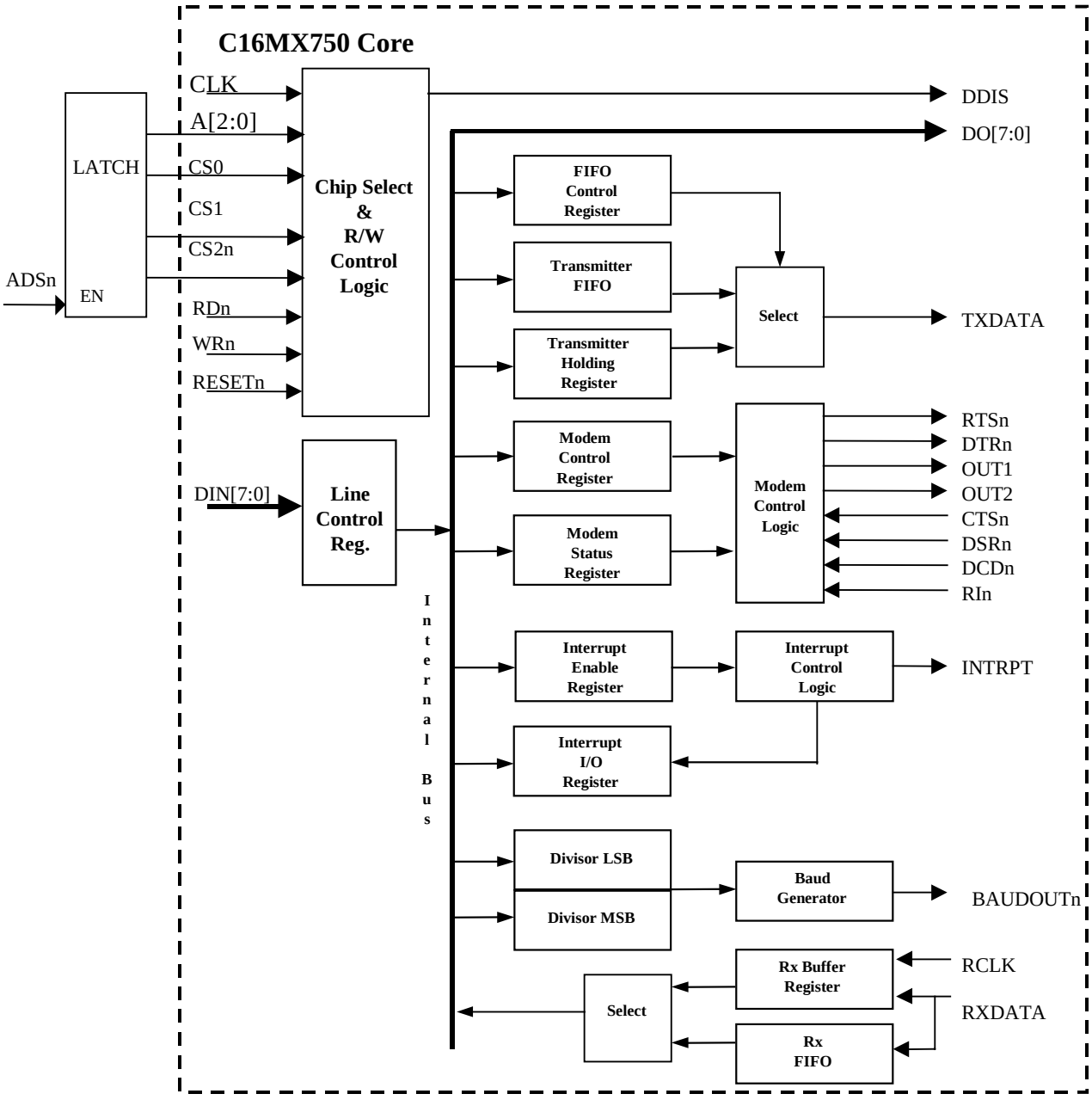


Figure 1: C16MX750 UART Block Diagram

Functional Description

Bit No	REGISTER ADDRESS											
	0 DLAB= 0	0 DLAB= 0	0 DLAB= 0	2	2	3	4	5	6	7	0 DLAB= 1	1 DLAB= 1
	Receiver Buffer Register (Read Only)	Transmiter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL‡	DLM‡
0	Data Bit 0	Data Bit 0†	Enable Received Data Available Interrupt (ERBI)	0 when Interrupt Pending	FIFO Enable	Word Length Select Bit 0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty (ETBEI)	Interrupt ID Bit 1	Receiver FIFO Reset	Word Length Select Bit 1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit 2	Transmitter FIFO Reset	Number of Stop Bits	OUT1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit 2	DMA Mose Select	Parity Enable	OUT2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	Sleep Mode Enable §	0	Reserved	Even Parity Select	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	Low Power Mode Enable §	64 byte FIFO Enabled	64 byte FIFO Enable‡	Stick Parity	Flow Control Enable	Transmitter Holding Register (THRE)	Data Set Ready (DSR	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled	Receiver Trigger (LSB)	Break Control	IrDA Enable‡	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled	Receiver Trigger (MSB)	Divisor latch Access Bit (DLAB)	Enhance Enable‡	Error in Receiver FIFO	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

† Bt 0 is the least significant bit. It is the first bit serially transmitted or received.
‡ Access to DLAB LSB, MSB, FCR bit 5 and MSR bit 6 and 7 require LCR bit 7 =1 These bits are always 0 in C16450 mode
§ These bit are always 0. c16MX750 doesn't support sleep mode and low power mode.

450 Mode

After a hardware reset bit 0 of the FIFO Control Register ('FCR') is cleared, so that C16MX750 is compatible with the 16C450. The transmitter and receiver FIFOs (named as the 'Transmit Holding Register' and 'Receiver Holding Register' respectively) have a depth of one character. This is mentioned as 'Byte mode'. When FCR[0] is cleared, all other mode selection parameters are ignored.

550 Mode

After a hardware reset, writing a 1 to FCR[0] will increase the FIFO depth to 16, providing compatibility with 16C550 devices.

Enhanced 550 Mode

Enhanced mode can be chosen through the use of MCR(7) with DLAB = 1. With DLAB = 1 and if MCR(7) = 1, enhanced mode is selected. It will increase the FIFO size to 64, thus providing a 550 device with 64 deep FIFOs.

750 Mode

Writing a 1 to FCR[0] will increase the FIFO size to 16. In the same way of standard 16C750, the FIFO size can be further increased to 64 by writing a 1 to FCR[5]. Note that access to FCR[5] is protected by LCR[7]. I.e., to set FCR[5], software should first set LCR[7] to temporarily remove the guard. Once FCR[5] is set, the software should clear LCR[7] for normal operation. The 16MX750 additional features over the 16C550 are:

1. Deeper FIFOs
2. Automatic RTS/CTS flow control
3. Sleep mode of standard 16C750 is not supported by C16MX750

IrDA Mode

Infra-red "IrDA-format" transmit and receive mode.
(This mode is additional feature of C16MX750 over standard 16750 devices)
IR mode can be chosen through the use of MCR(6) with DLAB = 1. With DLAB = 1 and if MCR(6) = 1, IR mode is selected.
It can be used combined with any of previous modes.

Autoflow control

Auto-flow control is formed from auto-CTSn and auto-RTSn. With auto-CTSn, CTSn must be active before the transmit FIFO can transmit data (see Figure 2). With auto-RTSn, RTSn becomes active when the receiver is empty or the threshold has not been reached. When RTSn is connected to CTSn, data transmission does not occur unless the receive FIFO has empty space. In this way, overrun errors are eliminated when UART1 and UART2 are C16MX750 with enabled autoflow control. Otherwise, overrun errors occur if the transmit data rate exceeds the receive FIFO read latency.

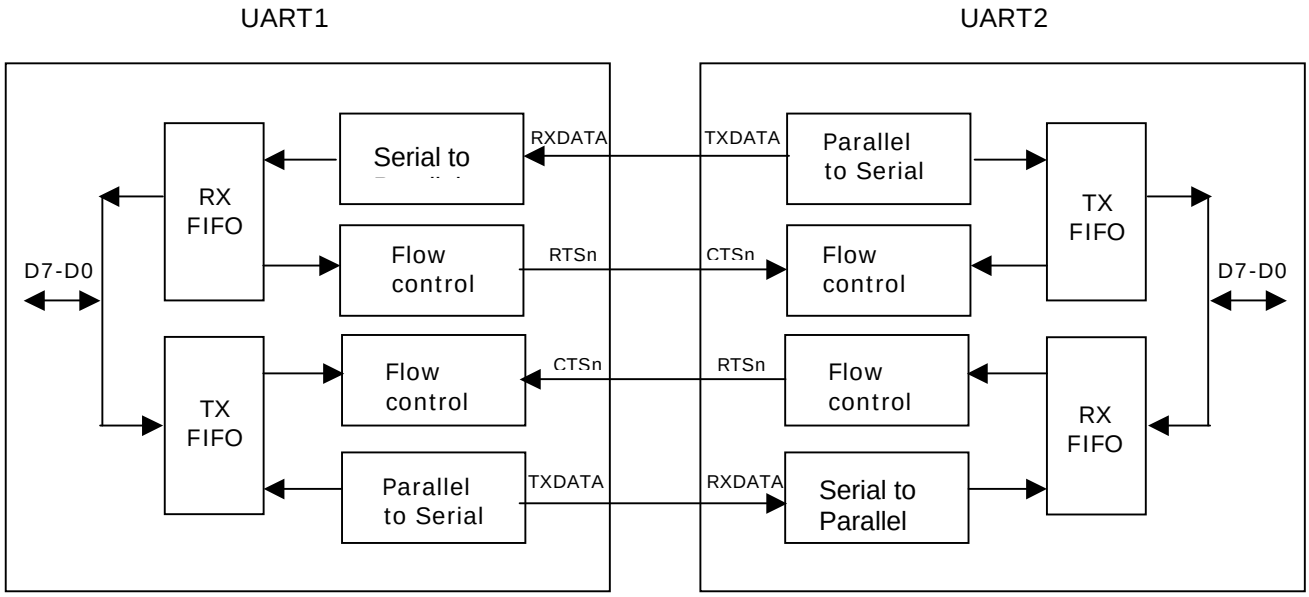


Figure 2 Autoflow Control (Auto-RTSn and Auto-CTSn)

auto-RTSn

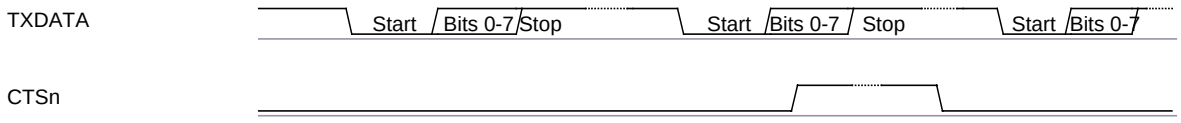
Auto-RTSn data flow control starts in the receiver timing and control block (see functional block diagram) and depends on the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger levelof 1, 4, 8, or 14 in 16-byte mode or 1, 16, 32, or 56 in 64-byte mode, RTSn is deasserted. The sending UART may send an additional byte after the trigger level is reached (in case the sending UART has another byte to send) because it may not recognize the deassertion of RTSn until after it has begun sending the additional byte. RTSn is automatically reasserted once the receiver FIFO is emptied by reading the receiver buffer register. The reassertion signals the sending UART to continue transmitting data.

auto-CTSn

The transmitter section checks CTSn before sending the next data byte. When CTSn is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, CTSn must be released before the middle of the last stop bit that is currently being sent. The auto-CTSn function reduces interrupts to the host system. When flow control is enabled, the CTSn state changes and does not trigger host interrupts because the device automatically controls its own transmitter. Without auto-CTSn, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result.

enabling auto-RTSn and auto-CTSn

The auto-RTS and auto-CTS modes of operation are activated by setting bit 5 of the modem control register (MCR) to 1



CTSn Functional Timing

NOTES: A. When CTSn is low, the transmitter starts sending serial data out.
B. When CTSn goes high before the middle of the last stop bit of the current byte, the transmitter stops sending the current byte but it does not send the next byte.
C. When CTSn goes from high to low, the transmitter begins sending data again.

The receiver FIFO trigger level can be set to 1, 4, 8, or 14 bytes for the 16-byte mode and 1, 16, 32, or 56 bytes for 64-byte mode

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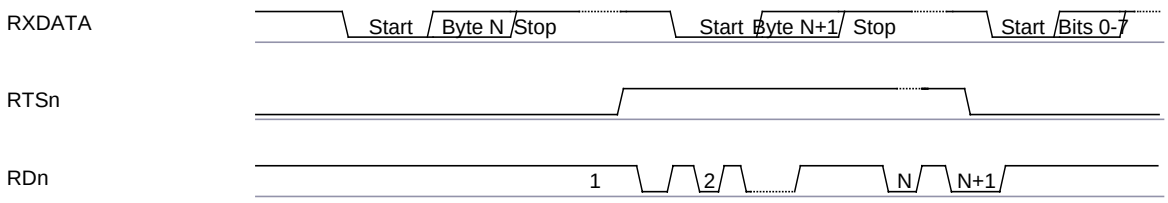


RTSn Functional Timing

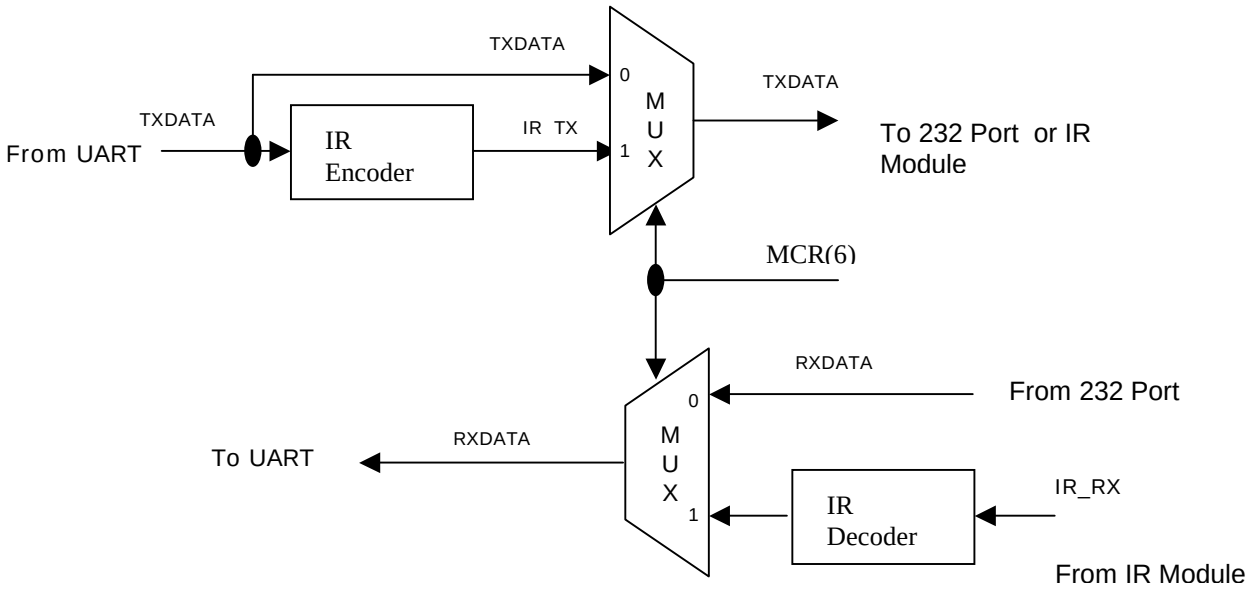
NOTES: A. N = receiver FIFO trigger level

B. The two blocks in dashed lines cover the case where an additional byte is sent as described in auto-RTSn.

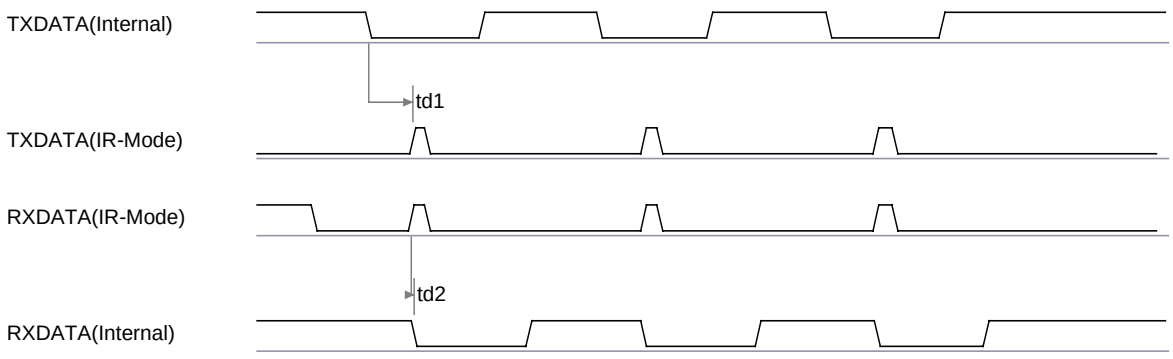
OPTIONAL IrDA codec

The IR encoder and decoder circuitry work with the UART to convert the serial bit stream into a series of pulses and back again. For every zero bit in the serial stream, a pulse is sent at the middle of the bit with a duration of 3/16 of a bit time. If a one or series of ones is sent, the encode does not send a pulse. The decoding process consists of receiving a pulse and sending a longer pulse to the UART. The wider pulse must be at least three-fourths of a bit time to be correctly decoded by most UARTs. Because the serial stream can occur at any baud rate, some way of changing the encoding and decoding baud rate is necessary. The easiest way to do this is to clock the encoder and decoder circuits with the UART baud rate 16x clock.

IR mode can be chosen through the use of MCR(6) with DLAB = 1. With DLAB = 1 and if MCR(6) = 1, IR mode is selected. Built in multiplexers are used to select the correct signal to input to the UART.



For encoding, the IR_TX is selected when MCR6 is set to 1. This sends IR_TX on the device TXDATA pin.
This signal can be used as an input to any IR transceiver .
For decoding, the IR_RX from the device (this can be connected to any IR transceiver) goes through the IR decode block and then it is the input to the UART .



IR Signal Transfer

Line Control (LCR)

The Line Control Register is used to specify the data communication format. The break feature, parity, stop bits and word length can be changed by writing to the appropriate bits in LSR.

Line Status (LSR)

This register provides information on the status of data transfers between the C16550 and the CPU.

Interrupt Enable (IER)

The Interrupt Enable Register masks interrupts from the modem status registers, line status, transmitter empty and receiver ready to the INTRPT output pin.

Modem Status (MSR)

This register provides the current state of modem control lines.

Modem Control (MCR)

This register controls the interface lines with the MODEM and changes the status of the C16550 from normal operating mode and local loop-back mode (diagnostics mode).

Transmitter Holding Buffer

The transmitter section is composed of a Transmit Holding Register (THR) and a Transmit Shift Register (TSR). Writing to THR will transfer the contents of the data bus (DIN 7-0) to the Transmit Holding Register every time that the THR or TSR is empty. This write operation should be done when Transmit Holding Register Empty (THRE) is set.

Receiver Buffer

This register contains the assembled received data. On the falling edge of the start bit, the receiver section starts its operations. The start bit is valid if the RXDATA is still low at the middle sample of Start bit, thus preventing the receiver from assembling a false data character.

Interrupt Identification (IIR)

The Interrupt Identification Register provides the source of interrupt among four levels of prioritized interrupt conditions in order to minimize the CPU overhead during data transfers.

FIFO control register (FCR)

The FCR is a write-only register at the same location as the IIR, which is a read-only register. The FCR enables the FIFOs, clears the FIFOs, sets the receiver FIFO trigger level, and selects the type of DMA signaling.

Scratchpad (SR)

This register stores the temporary byte for variable use.

Megafunction Assumptions

The functionality of the C16MX750 megafunction was based on the Texas Instruments TL16C550A. The following characteristics differentiate the C16MX750 from the Texas Instruments device:

- This megafunction does not support connection of a crystal directly to the device. It was replaced by an external master clock signal (CLK).
- The bi-directional data bus has been split into two separate buses: DIN[7:0] and DO[7:0]. If required these buses can be combined into a single 8-bit bi-directional bus.
- The 1½ stop bit mode (for 5-bit word length) is not supported.
- Signals rd2, wr2, xin and xout have been eliminated from the interface.
- Signal ADSn and address latch have been removed.
- Divisor latch low (DLL), divisor latch high (DLM), THR register and SCR register are reset to all zeros.
- Both DLL and DLM registers must be loaded before BAUDOUTn has valid output.
- DO (output data bus) always shows the last selected register; after reset DO is "00".
- MSR register is reset during the clock cycle following a MSR read.
- Transmitter Empty status (TEMT), bit 6 of Line Status Register (LSR), is reset during the clock cycle following a TBR register write.
- Between 2 rising edges of WRn or RDn the megafunction needs at least 2 clock (CLK) cycles. (Tcycle)
- Register Selectable Sleep Mode and Low-Power Mode are NOT SUPPORTED

Timing variations differences from the Texas Instruments device:

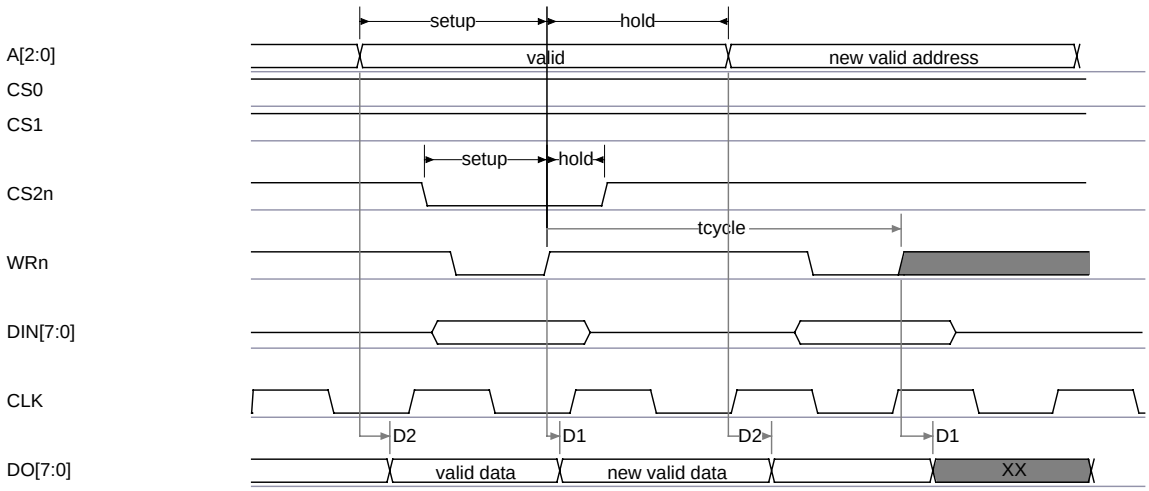
Symbol	Parameter	C16MX750		TL16C550A	
		Min	Max	Min	Max
td_1	Delay from WRn MCR to Output		tpd		100 ns
td_2	Delay from MODEM Input to Set Interrupt		2 CLK Cycles		170 ns
td_3	Delay from RDn to Reset Interrupt(RD MDR)		tpd after first CLK rising edge		140 ns
td_4	Delay from WRn to Reset Interrupt(WR THR)		2 CLK Cycles		140 ns
td_5	Delay from RDn to Reset Interrupt THRE (RD IIR)		tpd		140 ns
td_6	Delay from initial INTR Reset to Transmit Start	1 Baudout Cycles	4 Baudout Cycles	8 Baudout Cycles	24 Baudout Cycles
td_7	Delay from initial Write to Interrupt	4 Baudout Cycles	4 Baudout Cycles	16 Baudout Cycles	32 Baudout Cycles
td_8	Delay from STOP to Interrupt (THRE)	1 CLK Cycle	1 CLK Cycle	8 Baudout Cycles	8 Baudout Cycles
td_9	Delay from START to TXRDYn active		1 CLK Cycle		8 Baudout Cycles
td_{10}	Delay from Write to TXRDYn inactive	1 CLK Cycle	2 CLK Cycles		195 ns

td_{11}	Delay from STOP to Set Interrupt		tpd		1-3 RCLK Cycles
td_{12}	Delay from RD RBR to RXRDYn inactive		tpd		150 ns
td_{13}	Address, ADSn, Chip Select setup time [1]			15 ns	
td_{14}	Address, ADSn, Chip Select hold time [1]			5 ns	

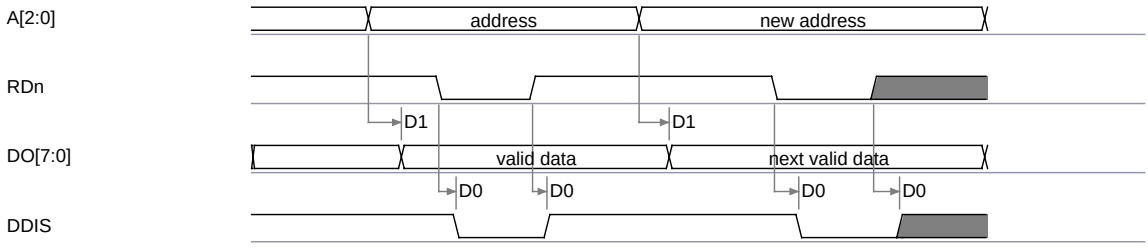
[1] Typical values: silicon dependent

All delays : setup, hold, D0, D1, D2 are silicon dependent

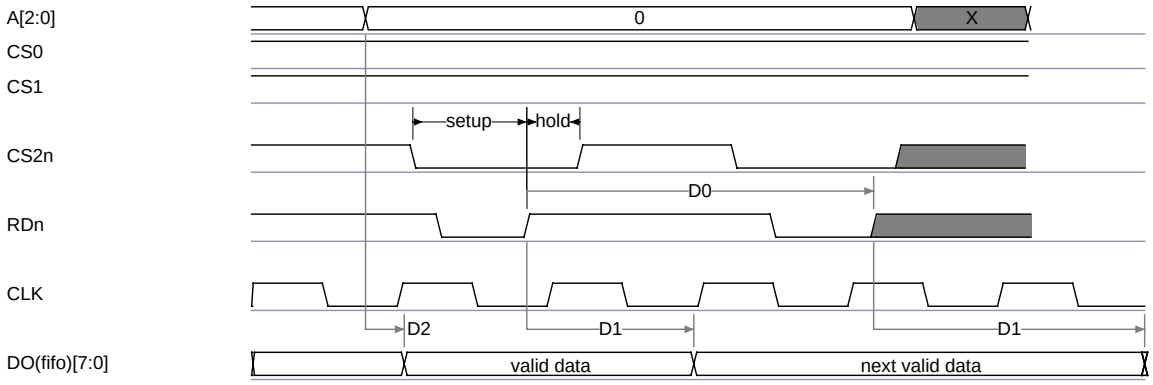
Timing Diagrams



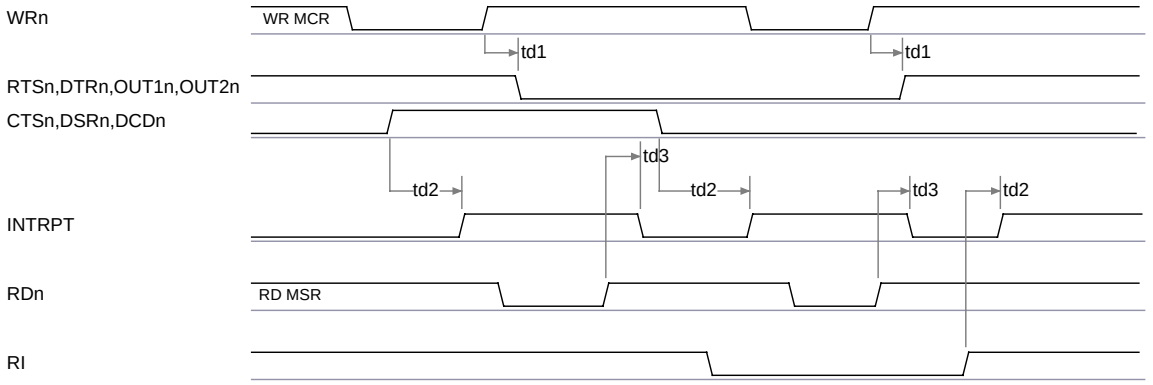
Write Cycle Timing



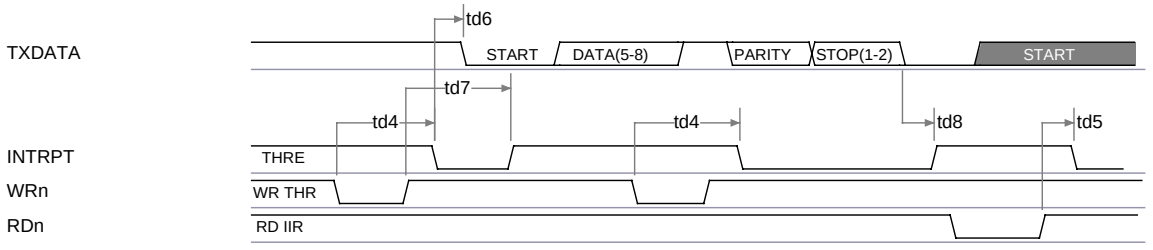
Read Cycle Timing



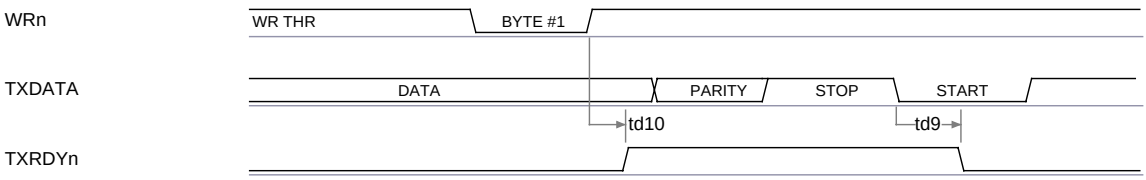
Read of FIFO Timing



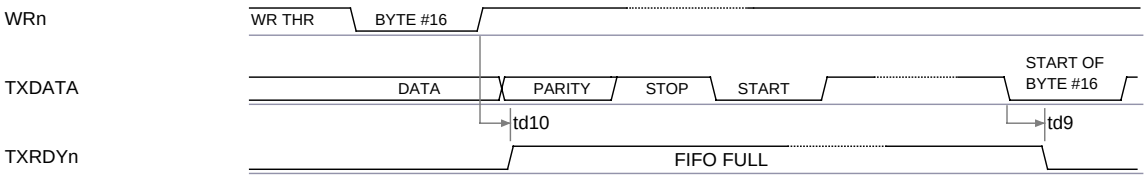
MODEM Control Timing



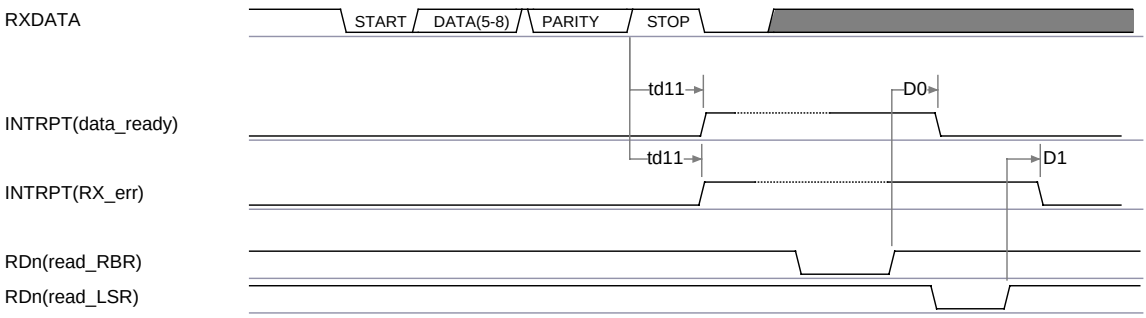
Transmitter Timing



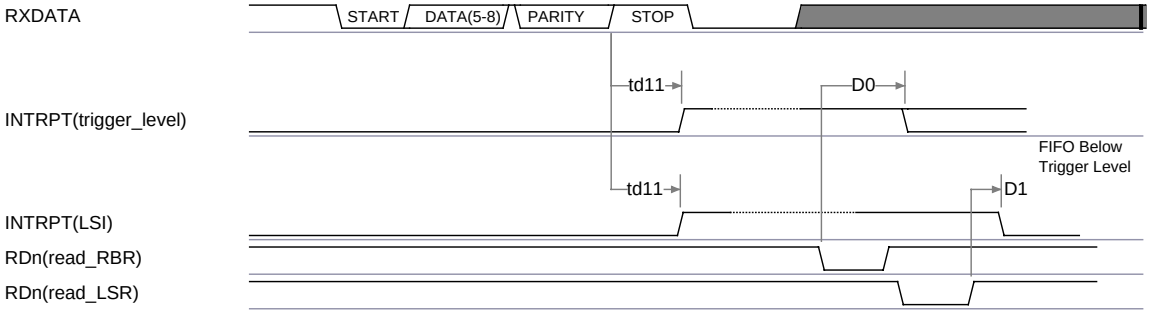
Transmitter Ready, FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



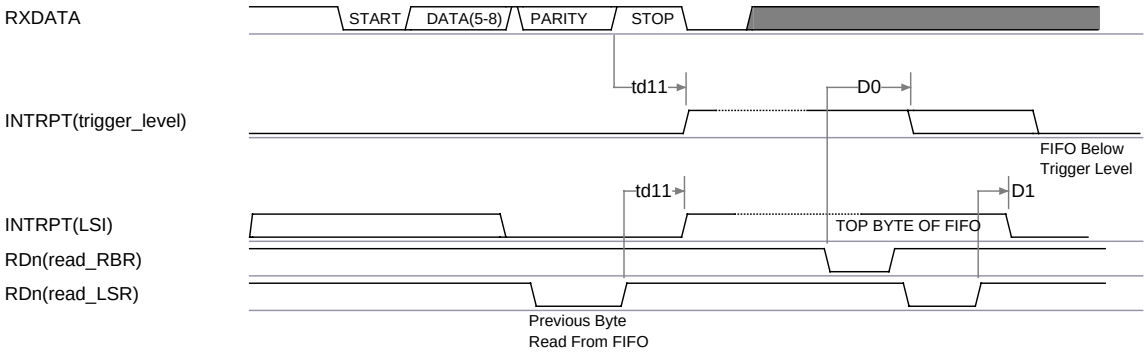
Transmitter Ready, FCR0 = 1 and FCR3 = 1 (Mode 1)



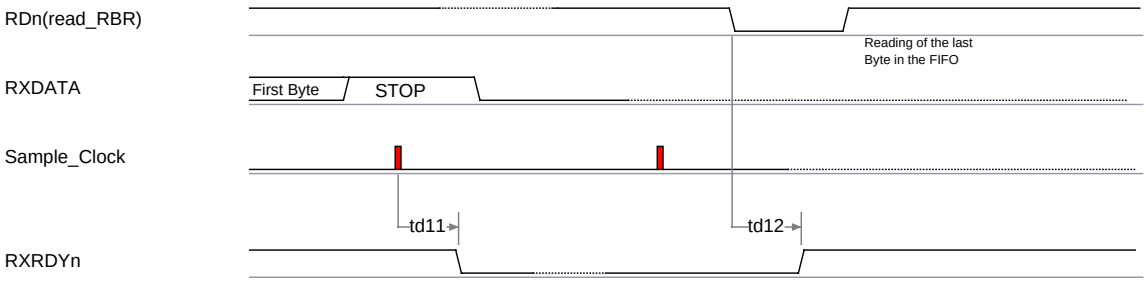
Receiver Timing



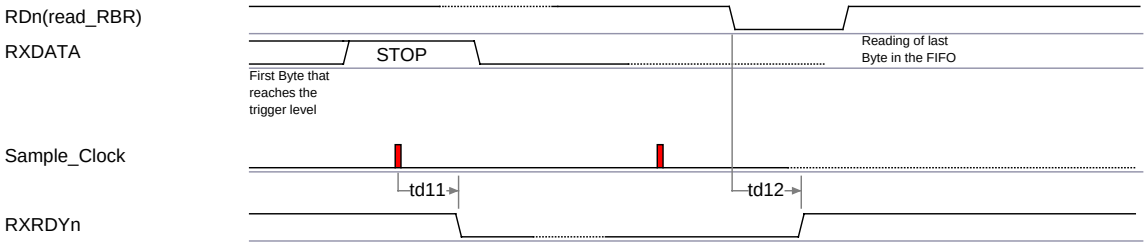
Receiver FIFO first Byte(Sets DR bit)



Receiver FIFO other than first Byte(DR internal bit already set)



Receiver Ready, FCR0 =0 or FCR0=1 and FCR3 = 0 (Mode 0)



Receiver Ready, FCR0 =1 and FCR3 = 1 (Mode 1)

Device Utilization & Performance

Target Device	Speed Grade	Utilization		Performance F_{max}	Availability
		LCs	EABs		
EPF10K100E	-1	648	2	45 MHz	**Now**
EP1K30	-1	648	2	46 MHz	**Now**
EP20K60	-1	627	2	76 MHz	**Now**

Deliverables

Encrypted Licenses

- Post-synthesis AHDL or EDIF
- Assignment & Configuration
- Symbol file
- Include file
- Vectors for testing the functionality of the megafunction

HDL Source Licenses

- VHDL or Verilog RTL source code
- Testbench
- Vectors for testbench
- Expected results for testbench
- Simulation script
- Synthesis script

Related Information

Data Transmission Circuits 1993 Data Book
Contact:
Texas Instruments
Literature Response Center
P.O. Box 809066
Dallas, Texas 75380-9066
URL: http://www.ti.com

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E-Mail: info@cast-inc.com
URL: www.cast-inc.com

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