C16550
Universal Asynchronous Receiver/Transmitter with FIFOs

Function Description

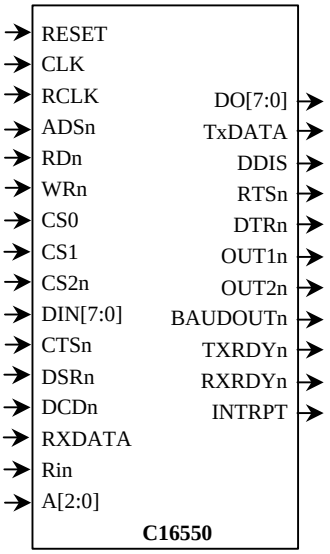
The C16550 programmable asynchronous communications interface (UART) megafunction provides data formatting and control to a serial communication channel.

The megafunction has select, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting asynchronous operation.

Features

- Capable of running with all existing 16450 and 16550A Software
- Asynchronous operation
- In FIFO mode, Transmitter and Receiver are each buffered with 16-byte FIFOs to reduce the number of interrupts of the CPU
- Programmable data word length (5 - 8 bit), parity and stop bits
- Parity, overrun and framing error checking
- Supports up to 1.5 Mbps transmission rates
- Programmable Baud Rate Generator allows division of any reference clock by 1 to (2^{16}-1) and generates an internal 16 X Clock
- False start bit detection
- Automatic break generation and detection
- Internal diagnostic capabilities
- Peripheral modem control functions

Symbol



Pin Description

Name	Type	Polarity	Description
RESET	In	High	External reset
CLK	In	-	Master clock
RCLK	In	-	Receive clock
ADSn	In	Low	Address strobe
RDn	In	Low	Read control
WRn	In	Low	Write control
CS0	In	High	Chip Select 0
CS1	In	High	Chip Select 1
CS2n	In	Low	Chip Select 2
DIN[7:0]	In	-	Data Input Bus
CTSn	In	Low	Clear-to -Send
DSRn	In	Low	Data Set Ready
DCDn	In	Low	Data Carrier Detect
RXDATA	In	-	Receive Data
RIn	In	Low	Ring Indicator
A[2:0]	In	-	Register Select
D0[7:0]	Out	-	Data Output Bus
TXDATA	Out	-	Transmit Data
DDIS	Out	High	Driver Disable
RTSn	Out	Low	Request-to-Send
DTRn	Out	Low	Data Terminal Ready
OUT1n	Out	Low	Output 1
OUT1n	Out	Low	Output 2
TxRDYn	Out	Low	Transmit ready
RxRDYn	Out	Low	Receiver ready
INTRPT	Out	High	Interrupt
BAUDOUTn	Out	Low	Baud Out

Register description

The C16550 contains the following registers:

1. Line Control
2. Line Status
3. Interrupt Enable
4. Modem status
5. Modem Control
6. Transmitter Holding buffer
7. Receiver buffer
8. Interrupt Identification
9. Scratch

Block Diagram

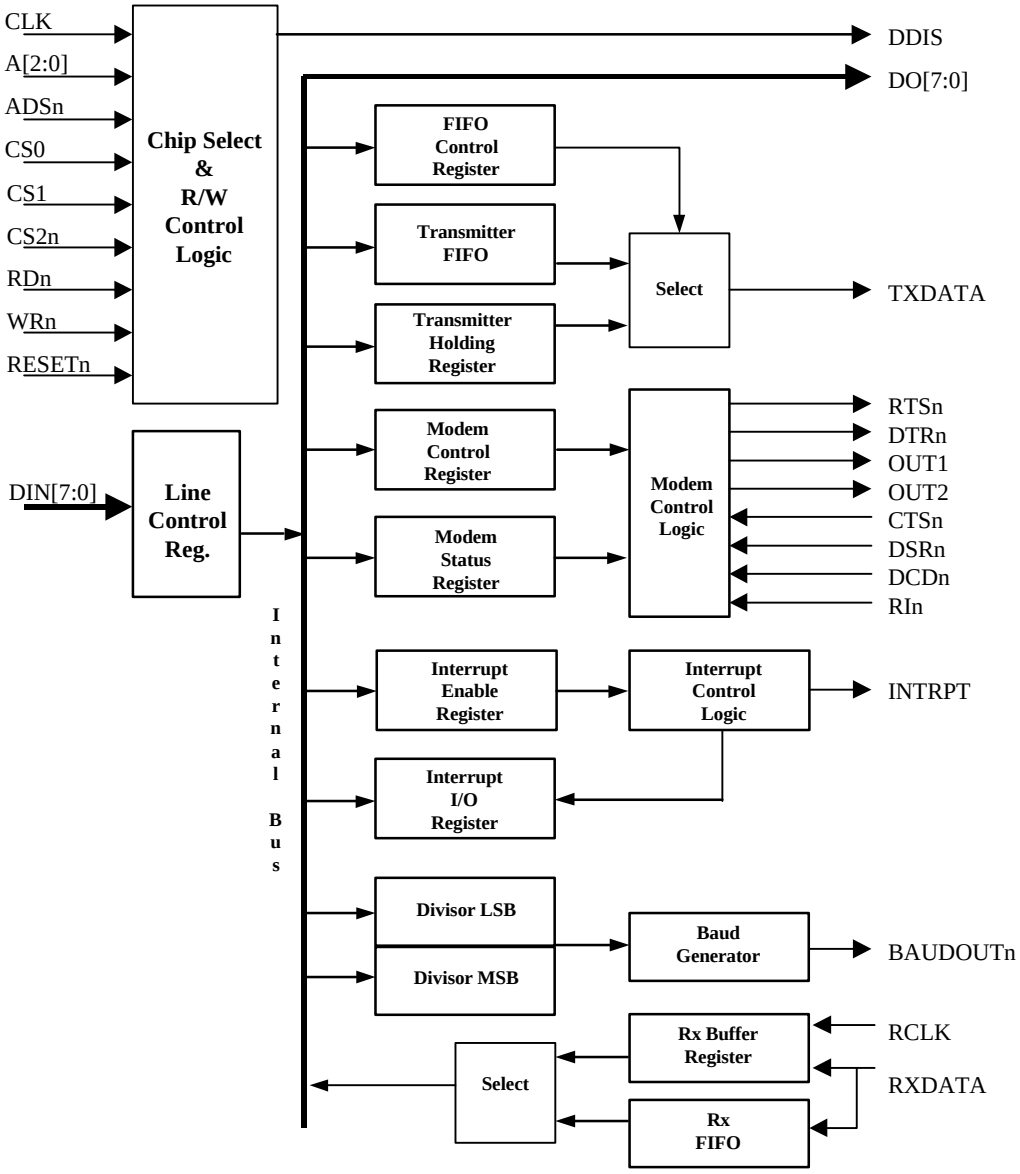


Figure 1: C16550 UART Block Diagram

Applications

- Serial data communications applications
- Modem interface

Functional Description

Line Control (LCR)

The Line Control Register is used to specify the data communication format. The break feature, parity, stop bits and word lenght can be changed by writing to the appropriate bits in LSR.

Line Status (LSR)

This register provides information on the status of data transfers between the C16550 and the CPU.

Interrupt Enable (IER)

The Interrupt Enable Register masks interrupts from the modem status registers, line status, transmitter empty and receiver ready to the INTRPT output pin.

Modem Status (MSR)

This register provides the current state of modem control lines.

Modem Control (MCR)

This register controls the interface lines with the MODEM and changes the status of the C16550 from normal operating mode and local loop-back mode (diagnostics mode).

Transmitter Holding Buffer

The transmitter section is composed of a Transmit Holding Register (THR) and a Transmit Shift Register (TSR). Writing to THR will tranfer the contents of the data bus (DIN 7-0) to the Transmit Holding Register every time that the THR or TSR is empty. This write operation should be done when Transmit Holding Register Empty (THRE) is set.

Receiver Buffer

This register contains the assembled received data. On the falling edge of the start bit, the receiver section starts its operations. The start bit is valid if the RXDATA is still low at the middle sample of Start bit, thus preventing the receiver from assembling a false data character.

Interrupt Identification (IIR)

The Interrupt Identification Register provides the source of interrupt among four levels of prioritized interrupt conditions in order to minimize the CPU overhead during data transfers.

Scratchpad (SR)

This register stores the temporary byte for variable use.

Device Utilization & Performance

Target Device	Speed Grade	Utilization		Performance	Availability
		LCs	EABs	F_{max}	
EPF10K20	-3	1079	-	25 MHz	**Now**
EPF10K30A	-1	1079	-	35 MHz	**Now**
EPF10K100B	-1	1079	-	40 MHz	**Now**
EPF10K30E	-1	656	2	47 MHz	**Now**
EP20K60	-1	1075	-	65 MHz	**Now**
EP1K30	-1	677	2	40 MHz	**Now**
EP1K30	-1	1136	-	63 MHz	**Now**

Deliverables

Encrypted Licenses

- Post-synthesis AHDL
- Assignment & Configuration
- Symbol file
- Include file
- Graphic Design file of test circuit
- Vectors for testing the functionality of the megafunction

VHDL Source Licenses

- VHDL RTL source code
- Testbench
- Example testbench wrapper for post-route simulation
- Vectors for testbench
- Simulation script
- Synthesis script
- Expected results for testbench

CAST, Inc.

24 White Birch Drive
Pomona, New York 10907 USA
Phone: +1 914-354-4945
Fax: +1 914-354-0325
E-Mail: info@cast-inc.com
URL : www.cast-inc.com

The C16550 megafunction is licensed from Moxsyn S.r.l.